Model Curriculum

QP Name: VLSI Design Engineer

QP Code: ELE/Q1201

QP Version: 4.0

NSQF Level: 5

Model Curriculum Version: 4.0

Electronics Sector Skills Council of India || 155, 2nd Floor, ESC House, Okhla Industrial Area - Phase 3, New Delhi – 110020

Table of Contents

Training Parameters

Sector	Electronics
Sub-Sector	Semiconductor & Components
Occupation	Product Design-S&C
Country	India
NSQF Level	5
Aligned to NCO/ISCO/ISIC Code	NCO-2015/2152.0501
Minimum Educational Qualification and Experience	Completed 2nd year of UG (UG Diploma) (Physics/Electronics/ Electrical/Mechanical) with 1.5 years of Relevant Experience OR Completed 3 year diploma after 10th (Electronics/Electrical/ Mechanical) with 3 Years of Relevant Experience OR Certificate-NSQF (Level 4.5) with 1.5 years of Relevant Experience # Relevant Experience in Semiconductor & Components.
Pre-Requisite License or Training	NA
Minimum Job Entry Age	18 Years
Last Reviewed On	01.05.2025
Next Review Date	30.04.2028
NSQC Approval Date	08.05.2025
QP Version	4.0
Model Curriculum Creation Date	01.05.2025
Model Curriculum Valid Up to Date	30.04.2028
Model Curriculum Version	4.0
Minimum Duration of the Course	570 Hours
Maximum Duration of the Course	570 Hours

Program Overview

This section summarizes the end objectives of the program along with its duration.

Training Outcomes

At the end of the program, the learner should have acquired the listed knowledge and skills.

- Memorize the basic concepts of system designing and computer architecture.
- Perform designing of function of SOC module of IC.
- Achieve productivity and quality standards for the correct specification output.
- Interact and coordinate with the supervisor and colleagues etc.
- Follow safe and healthy work practices.

Compulsory Modules

The table lists the modules and their duration corresponding to the Compulsory NOS of the QP.

NOS and Module Details	Theory Duration	Practical Duration	On-the-Job Training Duration (Mandatory)	On-the-Job Training Duration (Recommended)	Total Duration
ELE/N1427: Developing Functional Design for SOC Modules	**96:00**	**114:00**	**90:00**	**00:00**	**300:00**
Module 1: Developing Functional Design for SOC Modules	96:00	114:00	90:00	00:00	300:00
ELE/N1428: Coordinating and Implementing SOC Design Verification and Testing	**60:00**	**60:00**	**90:00**	**00:00**	**210:00**
Module 2: Coordinating and Implementing SOC Design Verification and Testing	60:00	60:00	90:00	00:00	210:00
DGT/VSQ/N0102- Employability Skills (60 Hours)	**24:00**	**36:00**	**00:00**	**00:00**	**60:00**
Module 3: Employability Skills (60 Hours)	24:00	36:00	00:00	00:00	60:00
Total Duration	**180:00**	**210:00**	**180:00**	**00:00**	**570:00**

Module Details

Module 1: Developing Functional Design for SOC Modules

Mapped to ELE/N1427

Terminal Outcomes:

- Recall the basics of digital electronics and computer architecture.

Duration: *96:00*	**Duration**: *114:00*
Theory – Key Learning Outcomes	**Practical – Key Learning Outcomes**
• Learn the fundamentals of System on Chip (SoC) architecture, including components like CPUs, memory, peripherals, and interconnects. • Study the various functional design approaches, such as top-down and bottom-up methodologies, and their relevance in SoC module development. • Gain theoretical knowledge of HDLs such as Verilog or VHDL used to describe digital logic at various levels of abstraction. • Learn about simulation models, test benches, and formal verification to validate the functionality of SoC modules before implementation. • Study the impact of design decisions on power consumption, performance, and chip area, and how to optimize them.	• Write and test Verilog/VHDL code for functional blocks like ALUs, memory controllers, and bus interfaces. • Draft and review design specifications that detail the required functionality, interfaces, and constraints for SoC modules. • Work with tools like ModelSim, Vivado, or Synopsys to simulate and debug functional designs. • Implement the designed module into a larger SoC system and ensure its correct functionality via integration testing. • Apply techniques to refine HDL designs to meet specific PPA goals, balancing trade-offs in power, speed, and silicon area.
Classroom Aids:	
Whiteboard, marker pen, computer or laptop attached to LCD projector, scanner, computer speakers	
Tools, Equipment and Other Requirements	
Server, switch, leased line, UPS, air Conditioning, server software, system software, Cadence/Synopsys/Mentor Design Suite , xManager or VNC Viewer	

Module 2: Coordinating and Implementing SOC Design Verification and Testing

Mapped to ELE/N1428

Terminal Outcomes:

- Identify the requirements for designing function of SOC module.
- Perform steps to carry out designing of function of SOC module.

Duration: *60:00*	**Duration**: *60:00*
Theory – Key Learning Outcomes	**Practical – Key Learning Outcomes**
• Learn the use of hardware description languages (e.g., Verilog, VHDL) and high-level languages in modeling, simulation, and design of SoC components. • Understand how to identify, evaluate, and integrate IP core blocks in SoC systems and how to define system behavior based on architectural inputs. • Learn about different types of design representations: high-level design, control logic, memory interfaces, and how to translate them into HDL. • Gain knowledge of structuring digital logic systems including data paths, control units, and interconnect strategies. • Study the methodology of verification, coverage metrics, assertion-based verification, and the role of physical design and DFT teams in design closure	• Write, simulate, and debug hardware descriptions using Verilog/VHDL for specific SoC components. • Build accurate simulation models (e.g., VHDL) of the system and validate them against behavioral specifications. • Design logic including control structures, data paths, and interconnects, and represent them using schematics or HDL. • Collaborate with verification engineers, evaluate simulation outcomes, and recommend design updates. • Work with physical design and DFT engineers to incorporate design-for-test features and optimize based on verification feedback.
Classroom Aids:	
Whiteboard, marker pen, computer or laptop attached to LCD projector, scanner, computer speakers	
Tools, Equipment and Other Requirements	
Server, switch, leased line, UPS, air Conditioning, server software, system software	

Module 3: Employability Skills (60 Hours)

Mapped to DGT/VSQ/N0102

Terminal Outcomes:

- Discuss about Employability Skills in meeting the job requirements
- Describe opportunities as an entrepreneur.
- Describe ways of preparing for apprenticeship & Jobs appropriately.

Duration: 24:00	Duration: 36:00
Theory – Key Learning Outcomes	**Practical – Key Learning Outcomes**
• Explain constitutional values, civic rights, responsibility towards society to become a responsible citizen • Discuss 21st century skills • Explain use of basic English phrasesand sentences. • Demonstrate how to communicate ina well-behaved manner • Demonstrate how to work withothers • Demonstrate how to operate digitaldevices • Discuss the significance of Internetand Computer/ Laptops • Discuss the need for identifyingbusiness opportunities • Discuss about types of customers. • Discuss on creation of biodata • Discuss about apprenticeship andopportunities related to it.	• List different learning and employability related GOI andprivate portals and their usage • Show how to practice different environmentally sustainable practices. • Exhibit 21st century skills like Self-Awareness, Behavior Skills, time management, etc. • Show how to use basic English sentences for everyday conversation in different contexts, in person and over the telephone • Demonstrate how to communicate in a well-mannered way with others. • Demonstrate how to communicate effectively using verbal and nonverbal communication etiquette • Utilize virtual collaboration tools to work effectively • Demonstrate how to maintain hygiene and dressing appropriately. • Perform a mock interview
Classroom Aids	
Training Kit (Trainer Guide, Presentations). Whiteboard, Marker, Projector, Laptop	
Tools, Equipment and Other Requirements	
Computer, UPS, Scanner, Computer Tables, LCD Projector, Computer Chairs, White BoardOR Computer Lab	

Module 4: On-the-Job Training

Mapped to VLSI Design Engineer

Mandatory Duration: *180:00*	**Recommended Duration**: *00:00*
Location: On Site	

Terminal Outcomes

1. Explain the fundamental concepts of electronics and electronics components
2. Select the appropriate coding for designing the module.
3. Co-ordinate with different design teams for specifying and designing the function of system blocks.
4. Specify the external interfaces, behavioral requirements for the design and tasks to be performed by the module of the chip.
5. Use HDL for writing the hardware description of IC.
6. Build a simulated model, e.g. VHDL model for ASIC design as per the system specification.
7. Identify the requirements for designing function of SOC module.
8. Perform designing of function of SOC module
9. Interact and coordinate with supervisor and colleagues
10. Work as per the given timeline and quality standards
11. Maintain a safe, healthy and secure work environment

Annexure

Trainer Requirements

Trainer Prerequisites						
Minimum Educational Qualification	**Specialization**	**Relevant Industry Experience**		**Training Experience**		**Remarks**
		Years	***Specialization***	***Years***	***Specialization***	
Diploma/ Graduate / Certified in relevant CITS Trade	Electronics	3	VLSI Design Engineer	2	Trainer	

Trainer Certification	
Domain Certification	**Platform Certification**
"**VLSI Design Engineer**, ELE/Q1201, version 4.0". Minimum accepted score is 80%.	Recommended that the Trainer is certified for the **VLSI Design Engineer** "Trainer (VET and Skills)", mapped to the Qualification Pack: "MEP/Q2601, V2.0", with minimum score of 80%

Assessor Requirements

Assessor Prerequisites						
Minimum Educational Qualification	**Specialization**	**Relevant Industry Experience**		**Training/Assessment Experience**		**Remarks**
		Years	***Specialization***	***Years***	***Specialization***	
Diploma/ Graduate / Certified in relevant CITS Trade	Electronics	5	VLSI Design Engineer	2	Assessor	

Assessor Certification	
Domain Certification	**Platform Certification**
"**VLSI Design Engineer**, ELE/Q1201, version 4.0". Minimum accepted score is 80%.	Recommended that the Assessor is certified for the **VLSI Design Engineer** "Assessor (VET and Skills)", mapped to the Qualification Pack: "MEP/Q2701, V2.0", with minimum score of 80%

Assessment Strategy

1. Assessment System Overview:
    - Batches assigned to the assessment agencies for conducting the assessment on SDMS/SIP or email
    - Assessment agencies send the assessment confirmation to VTP/TC looping SSC
    - Assessment agency deploys the ToA certified Assessor for executing the assessment
    - SSC monitors the assessment process & records

2. Testing Environment:
    - Confirm that the center is available at the same address as mentioned on SDMS or SIP
    - Check the duration of the training.
    - Check the Assessment Start and End time to be as 10 a.m. and 5 p.m.
    - If the batch size is more than 30, then there should be 2 Assessors.
    - Check that the allotted time to the candidates to complete Theory & Practical Assessment is correct.
    - Check the mode of assessment—Online (TAB/Computer) or Offline (OMR/PP).
    - Confirm the number of TABs on the ground are correct to execute the Assessment smoothly.
    - Check the availability of the Lab Equipment for the particular Job Role.

3. Assessment Quality Assurance levels / Framework:
    - Question papers created by the Subject Matter Experts (SME)
    - Question papers created by the SME verified by the other subject Matter Experts
    - Questions are mapped with NOS and PC
    - Question papers are prepared considering that level 1 to 3 are for the unskilled & semi-skilled individuals, and level 4 and above are for the skilled, supervisor & higher management
    - Assessor must be ToA certified & trainer must be ToT Certified
    - Assessment agency must follow the assessment guidelines to conduct the assessment

4. Types of evidence or evidence-gathering protocol:
    - Time-stamped & geotagged reporting of the assessor from assessment location
    - Centre photographs with signboards and scheme specific branding
    - Biometric or manual attendance sheet (stamped by TP) of the trainees during the training period
    - Time-stamped & geotagged assessment (Theory + Viva + Practical) photographs & videos

5. Method of verification or validation:
    - Surprise visit to the assessment location
    - Random audit of the batch
    - Random audit of any candidate

6. Method for assessment documentation, archiving, and access
    - Hard copies of the documents are stored
    - Soft copies of the documents & photographs of the assessment are uploaded / accessed from Cloud Storage
    - Soft copies of the documents & photographs of the assessment are stored in the Hard Drives

References

Glossary

Sector	Sector is a conglomeration of different business operations having similar business and interests. It may also be defined as a distinct subset of the economy whose components share similar characteristics and interests.
Sub-sector	Sub-sector is derived from a further breakdown based on the characteristics and interests of its components.
Occupation	Occupation is a set of job roles, which perform similar/ related set of functions in an industry.
Job role	Job role defines a unique set of functions that together form a unique employment opportunity in an organization.
Occupational Standards (OS)	OS specify the standards of performance an individual must achieve when carrying out a function in the workplace, together with the Knowledge and Understanding (KU) they need to meet that standard consistently. Occupational Standards are applicable both in the Indian and global contexts.
Performance Criteria (PC)	Performance Criteria (PC) are statements that together specify the standard of performance required when carrying out a task.
National Occupational Standards (NOS)	NOS are occupational standards which apply uniquely in the Indian context.
Qualifications Pack (QP)	QP comprises the set of OS, together with the educational, training and other criteria required to perform a job role. A QP is assigned a unique qualifications pack code.
Unit Code	Unit code is a unique identifier for an Occupational Standard, which is denoted by an 'N'
Unit Title	Unit title gives a clear overall statement about what the incumbent should be able to do.
Description	Description gives a short summary of the unit content. This would be helpful to anyone searching on a database to verify that this is the appropriate OS they are looking for.
Scope	Scope is a set of statements specifying the range of variables that an individual may have to deal with in carrying out the function which have a critical impact on quality of performance required.

Knowledge and Understanding (KU)	Knowledge and Understanding (KU) are statements which together specify the technical, generic, professional and organisational specific knowledge that an individual needs in order to perform to the required standard.
Organizational Context	Organizational context includes the way the organization is structured and how it operates, including the extent of operative knowledge managers have of their relevant areas of responsibility.
Technical Knowledge	Technical knowledge is the specific knowledge needed to accomplish specific designated responsibilities.
Core Skills/ Generic Skills (GS)	Core skills or Generic Skills (GS) are a group of skills that are the key to learning and working in today's world. These skills are typically needed in any work environment in today's world. These skills are typically needed in any work environment. In the context of the OS, these include communication related skills that are applicable to most job roles.
Electives	Electives are NOS/set of NOS that are identified by the sector as contributive to specialization in a job role. There may be multiple electives within a QP for each specialized job role. Trainees must select at least one elective for the successful completion of a QP with Electives.
Options	Options are NOS/set of NOS that are identified by the sector as additional skills. There may be multiple options within a QP. It is not mandatory to select any of the options to complete a QP with Options.

Acronyms and Abbreviations

NOS	National Occupational Standard(s)
NSQF	National Skills Qualifications Framework
QP	Qualifications Pack
TVET	Technical and Vocational Education and Training
IPR	Intellectual Property Rights